CLAIMS

I/We claim:

Claims group

[c1] 1. A method of fabricating a memory cell on a workpiece having a substrate, a plurality of active areas in the substrate, and a dielectric layer over the active areas, the method comprising:

constructing bit line contact openings over a first portion of the active areas and cell plug openings over second portions of the active areas;

depositing a first conductive material into the bit line contact openings to form bit line contacts and into the cell plug openings to form cell plugs;

forming a trench through an upper portion of a plurality of the bit line contacts and portions of the dielectric layer, the trench having a first sidewall and a second sidewall;

fabricating a spacer along at least the first sidewall, the spacer being a dielectric material separate from the dielectric layer; and

fabricating a bit line in the trench, the bit line electrically coupling the bit line contacts and being electrically insulated from the cell plugs.

[c2] 2. The method of claim 1 wherein fabricating the bit line in the trench comprises using only two photolithographic and etching processes including (a) a first photolithographic and etching process to construct the bit line contact openings and the cell plug openings, and (b) a second photolithographic and etching process to form the trench through the upper portion of a plurality of bit line contacts.

[c3] 3. The method of claim 1 wherein fabricating the bit line in the trench comprises embedding the bit line in the dielectric layer so that the first and second sidewalls of the trench are between cell plugs.

[c4] 4. The method of claim 1 wherein fabricating the bit line in the trench comprises embedding the bit line in the dielectric layer and the bit line contacts so that (a) the first and second sidewalls of the trench are between cell plugs, and (b) the bit line has a top surface at least substantially coplanar with a top surface of the dielectric layer.

[c5] 5. The method of claim 1 wherein fabricating the bit line in the trench comprises superimposing the bit line over a shallow trench isolation structure but not over the first portion of the active areas.

[c6] 6. The method of claim 1 wherein:

constructing the bit line contact openings and the cell plug openings comprises (a) a first photolithographic process that forms a pattern on the dielectric layer having apertures corresponding to a desired arrangement of bit line contact openings, and (b) etching the dielectric layer to form the bit line contact openings; and

forming the trench comprises (a) a second photolithographic process that forms an elongated slot corresponding to a location for the trench, and (b) etching the trench in the upper portions of the bit line contacts and portions of the dielectric layer between the bit line contacts.

[c7] 7. The method of claim 1 wherein fabricating the spacer comprises (a) depositing a thin, conformal layer of a dielectric material onto the sidewalls and a bottom of the trench, and (b) removing the conformal dielectric material from the

bottom of the trench to open a bit line plug and electrically isolate adjacent cell plugs.

[c8] 8. The method of claim 1 wherein fabricating the spacer comprises (a) depositing a thin, conformal layer of a dielectric material onto the sidewalls and a bottom of the trench, and (b) removing the conformal dielectric material from the bottom of the trench without a mask layer.

[c9] 9. The method of claim 1 wherein fabricating the bit line comprises:

depositing a barrier layer in the trench;

depositing a second conductive layer over the barrier layer to fill the trench; and

planarizing the workpiece to remove an overburden portion of the first and second conductive layers relative to the dielectric layer.

[c10] 10. The method of claim 9 wherein the first conductive material comprises polysilicon, the barrier layer comprises tungsten nitride, and the second conductive material comprises tungsten.

[c11] 11. The method of claim 9 wherein the first conductive material comprises polysilicon, the barrier layer comprises tantalum, and the second conductive material comprises copper.

[c12] 12. A method of fabricating a component for a microelectronic device on a workpiece having a substrate, a plurality of active areas in the substrate, and a dielectric layer over the active areas, comprising:

forming a first pattern in a resist layer on the dielectric layer, the first pattern having an arrangement of apertures corresponding to a desired arrangement of bit line contact openings over first portions

of the active areas and cell plug openings over second portions of the active areas;

etching the dielectric layer to form bit line contact openings over the first portions of the active areas and cell plug openings over the second portions of the active areas;

depositing a first conductive material into the bit line contact openings to construct bit line contacts and into the cell plug openings to construct cell plugs;

forming a second pattern in another resist layer on the workpiece, the second pattern having an elongated slot extending over a plurality of the bit line contacts and portions of the dielectric layer;

etching an elongated trench in upper portions of the bit line contacts under the slot;

filling the elongated trench with a second conductive material; and

planarizing the workpiece to form a bit line in the elongated trench, bit line contacts in the dielectric layer, and cell plugs in the dielectric layer.

[c13] 13. The method of claim 12 wherein etching the trench comprises forming first and second sidewalls of the trench between cell plugs such that the bit line extends between the cell plugs.

[c14] 14. The method of claim 12 wherein etching the trench comprises forming first and second sidewalls of the trench between cell plugs, and planarizing the workpiece comprises forming a top surface on the bit line to be at least substantially coplanar with a top surface of the dielectric layer.

[c15] 15. The method of claim 12 wherein etching the trench comprises superimposing the trench over a shallow trench isolation structure but not over the first portion of the active areas.

[c16] 16. The method of claim 12, further comprising fabricating a spacer in the trench by depositing a thin, conformal layer of a dielectric material onto sidewalls and a bottom of the trench, and removing the conformal dielectric material from the bottom of the trench to open a bit line plug.

[c17] 17. The method of claim 12, further comprising depositing a barrier layer in the trench before depositing a second conductive layer into the trench, and then depositing the second conductive layer over the barrier layer to fill the trench.

[c18] 18. A method of fabricating a memory cell on a workpiece having a substrate, a plurality of active areas in the substrate, and a dielectric layer over the active areas, the method comprising:

constructing bit line contact openings over first portions of the active areas and cell plug openings over second portions of the active areas;

depositing a first conductive material into the bit line contact openings to form bit line contacts;

forming a trench through an upper portion of a plurality of bit line contacts and the dielectric layer, the trench having a first sidewall and a second sidewall; and

fabricating a bit line in the trench, the bit line electrically coupling selected bit line contacts and being electrically insulated from the cell plugs.

[c19] 19. The method of claim 18 wherein fabricating the bit line in the trench comprises using only two photolithographic and etching processes including (a) a first photolithographic and etching process to construct the bit line contact openings, and (b) a second photolithographic and etching process to form the trench through the upper portion of a plurality of bit line contacts.

[c20] 20. The method of claim 18 wherein fabricating the bit line in the trench comprises embedding the bit line in the dielectric layer so that the first sidewall and the second sidewall of the trench are between cell plugs to isolate cell plugs from bit lines.

[c21] 21. The method of claim 18 wherein fabricating the bit line in the trench comprises embedding the bit line in the dielectric layer and the bit line contacts so that (a) the first sidewall and the second sidewall of the trench are between cell plugs, and (b) the bit line has a top surface at least substantially coplanar with a top surface of the dielectric layer.

[c22] 22. The method of claim 18 wherein fabricating the bit line in the trench comprises superimposing the bit line over a shallow trench isolation structure but not over the first portion of the active areas.

[c23] 23. A method of fabricating circuitry for a memory cell formed on a workpiece having a substrate, a plurality of active areas in the substrate, and a dielectric layer over the active areas, the method comprising:

constructing bit line contact openings over first portions of the active areas and cell plug openings over second portions of the active areas in a first photolithographic procedure;

depositing a first conductive material into the bit line contact openings to form bit line contacts and into the cell plug openings to form cell plugs in a single deposition procedure;

forming a trench through an upper portion of a plurality of bit line contacts and the dielectric layer in a second photolithographic procedure; and

fabricating a bit line in the trench by depositing a second conductive material into the trench and planarizing the workpiece.

[c24] 24. The method of claim 23 wherein fabricating the bit line in the trench comprises using only the first and second photolithographic procedures.

[c25] 25. The method of claim 23 wherein fabricating the bit line in the trench comprises embedding the bit line in the dielectric layer so that a first sidewall and a second sidewall of the trench are between cell plugs.

[c26] 26. The method of claim 23 wherein fabricating the bit line in the trench comprises embedding the bit line in the dielectric layer and the bit line contacts so that (a) a first sidewall and a second sidewall of the trench are between cell plugs, and (b) the bit line has a top surface at least substantially coplanar with a top surface of the dielectric layer.

[c27] 27. The method of claim 23 wherein fabricating the bit line in the trench comprises superimposing the bit line over a shallow trench isolation structure but not over the first portion of the active areas.

[c28] 28. A method of fabricating circuitry for a memory cell formed on a workpiece having a substrate, a plurality of active areas in the substrate, and a dielectric layer over the active areas, the method comprising:

constructing bit line contact openings over first portions of the active areas and cell plug openings over second portions of the active areas in a first photolithographic procedure;

depositing a first conductive material into the bit line contact openings to form bit line contacts and into the cell plug openings to form cell plugs in a single deposition procedure;

forming a trench through an upper portion of a plurality of bit line contacts and the dielectric layer in a second photolithographic procedure; and

fabricating a bit line in the trench by depositing a second conductive material into the trench and planarizing the workpiece to an end point at which the bit line contact, the bit line, and the cell plugs have coplanar top surfaces.

[c29] 29. The method of claim 28 wherein fabricating the bit line in the trench comprises using only the first and second photolithographic procedures.

[c30] 30. The method of claim 28 wherein fabricating the bit line in the trench comprises embedding the bit line in the dielectric layer so that a first sidewall and a second sidewall of the trench are between cell plugs.

[c31] 31. The method of claim 28 wherein fabricating the bit line in the trench comprises embedding the bit line in the dielectric layer and the bit line contacts so that a first sidewall and a second sidewall of the trench are between cell plugs.

[c32] 32. The method of claim 28 wherein fabricating the bit line in the trench comprises superimposing the bit line over a shallow trench isolation structure but not over the first portion of the active areas.

[c33] 33. A method of fabricating a component for a microelectronic device having a workpiece including a substrate, a plurality of active areas in the substrate, a plurality of shallow trench isolation structures in the substrate between active areas, a dielectric layer over the active areas, bit line contacts in the dielectric layer contacting a first portion of the active areas and a portion of an adjacent shallow trench isolation structures, and cell plugs in the dielectric layer contacting a second portion of the active areas, the method comprising:

embedding an elongated bit line in a trench extending through an upper portion of the bit line contacts and sections of the dielectric layer between the bit line contacts, the elongated bit line being

superimposed over portions of the shallow trench isolation structures but not over the first portion of the active areas; and

electrically insulating the bit line from cell plugs by providing dielectric spacers in the trench between the bit line and the cell plugs.

[c34] 34. A microelectronic device, comprising:

a workpiece including a substrate, a plurality of active areas in the substrate, and a dielectric layer over the active areas;

a plurality of bit line contacts in the dielectric layer contacting first portions of the active areas;

a plurality of cell plugs in the dielectric layer contacting second portions of the active areas; and

a bit line structure embedded in an upper portion of the bit line contacts and portions of the dielectric layer between the bit line contacts, the bit line structure comprising an elongated conductive bit line and a dielectric spacer between the conductive bit line and cell plugs adjacent to the bit line.

[c35] 35. The device of claim 34, further comprising a liner between the bit line and the dielectric spacer.

[c36] 36. The device of claim 34 wherein:

the bit line comprises tungsten; and

the device further comprises a tungsten nitride barrier layer between the tungsten bit line and the spacer.

[c37] 37. The device of claim 34 wherein:

the bit line comprises copper; and

the device further comprises a tantalum barrier layer between the copper bit line and the spacer.

[c38] 38. The device of claim 34 wherein:

the dielectric layer has a top surface; and

the bit line has a top surface coplanar with the top surface of the dielectric layer.

[c39] 39. The device of claim 34 wherein:

the device further comprises a shallow trench isolation structure adjacent to the first portion of the active areas; and

the conductive bit line is superimposed over a portion of the shallow trench isolation structure but not over the first active area.

[c40] 40. A microelectronic device, comprising:

a workpiece including a substrate, a plurality of active areas in the substrate, and a dielectric layer over the active areas, the dielectric layer having an upper surface;

a plurality of bit line contacts in the dielectric layer contacting first portions of the active areas;

a plurality of cell plugs in the dielectric layer contacting second portions of the active areas; and

a conductive, elongated bit line embedded in an upper portion of the bit line contacts and portions of the dielectric layer between the bit line contacts, wherein the bit line extends between cell plugs.

[c41] 41. The device of claim 40, further comprising:

a dielectric spacer between the bit line and the cell plugs; and

a liner between the bit line and the dielectric spacer.

[c42] 42. The device of claim 41 wherein:

the bit line comprises tungsten; and

the liner comprises a tungsten nitride barrier layer.

[c43] 43. The device of claim 41 wherein:

the bit line comprises copper; and

the liner comprises a tantalum barrier layer.

[c44] 44. The device of claim 40 wherein:

the dielectric layer has a top surface; and

the bit line has a top surface coplanar with the top surface of the dielectric layer.

[c45] 45. The device of claim 40 wherein:

the device further comprises a shallow trench isolation structure adjacent to the first portion of the active areas; and

the conductive bit line is superimposed over a portion of the shallow trench isolation structure but not over the first active area.

[c46] 46. A computer, comprising:

a bus;

a central processing unit coupled to the bus; and

a memory device coupled to the bus, the memory device having a cell comprising –

a plurality of active areas in the substrate, and a dielectric layer over the active areas;

a plurality of bit line contacts in the dielectric layer contacting first portions of the active areas;

a plurality of cell plugs in the dielectric layer contacting second portions of the active areas; and

a bit line structure embedded in an upper portion of the bit line contacts and portions of the dielectric layer between the bit line contacts, the bit line structure comprising an elongated conductive bit line and a dielectric spacer between the

conductive bit line and cell plugs adjacent to the conductive bit line.

[c47] 47. The computer of claim 46, further comprising a liner between the bit line and the dielectric spacer.

[c48] 48. The computer of claim 46 wherein:

the bit line comprises tungsten; and

the computer further comprises a tungsten nitride barrier layer between the tungsten bit line and the spacer.

[c49] 49. The computer of claim 46 wherein:

the bit line comprises copper; and

the computer further comprises a tantalum barrier layer between the copper bit line and the spacer.

[c50] 50. The computer of claim 46 wherein:

the dielectric layer has a top surface; and

the bit line has a top surface coplanar with the top surface of the dielectric layer.

[c51] 51. The computer of claim 46 wherein:

the computer further comprises a shallow trench isolation structure adjacent to the first portion of the active areas; and

the conductive bit line is superimposed over a portion of the shallow trench isolation structure but not over the first active area.

[c52] 52. A computer, comprising:

a bus;

a central processing unit coupled to the bus; and

a memory device coupled to the bus, the memory device having a cell comprising –

a workpiece including a substrate, a plurality of active areas in the substrate, and a dielectric layer over the active areas, the dielectric layer having an upper surface;

a plurality of bit line contacts in the dielectric layer contacting first portions of the active areas;

a plurality of cell plugs in the dielectric layer contacting second portions of the active areas;

a conductive, elongated bit line embedded in an upper portion of the bit line contacts and portions of the dielectric layer between the bit line contacts, the bit line extending between cell plugs; and

a dielectric spacer between the conductive bit line and cell plugs adjacent to the conductive line.